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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Stephen J. Billick

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EXAMINER

CONTINO, PAUL F

ART UNIT

PAPER NUMBER

2114

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/699,305

Applicant(s)

BILLICK ET AL.

Examiner

Paul Contino

Art Unit

2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 September 2006.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7, 10-12, 14-19, 21, 22 and 24-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 10-12, 14-19, 21, 22 and 24-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION: Final Rejection

Response to Arguments

1. Applicant's arguments pertaining to the prior art rejections, filed September 12, 2006, have been fully considered but they are not persuasive.

The Examiner respectfully disagrees with the Applicant with regard to the arguments pertaining to relinquishment and retention operations as not being equivalent to “disabling” a memory device, as in the second to last paragraph of page 11 of the Applicant’s Remarks. Though the Applicant regards relinquishment and retention as mutually exclusive operations, the invention as claimed offers alternative means of “disabling” a memory device, and therefore the mutually exclusive operations, when applied independent of one another, are interpreted as reading on the Applicant’s invention.

The Examiner respectfully disagrees with the Applicant with regard to the arguments pertaining to the interpretation of relinquishment as being a means of “disabling”, as in the last paragraph of page 11 of the Applicant’s remarks. It is inferred from the Schelling prior art reference that the relinquished memory (20b) is exclusively for use by the computer system to function while only the remaining memory (20a) is tested (Schelling: column 4 lines 3-13).

The Examiner respectfully disagrees with the Applicant with regard to the arguments pertaining to the affirmative operation of disabling memory as in the first paragraph of page 12 of the Applicant’s remarks. There is no reference in the claims to a prior “enablement” of memory, or to what “disabling” or “enabling” specifically entails.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 6, 10, 11, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Schelling (U.S. Patent No. 6,766,474).

As in claim 1, Schelling discloses software for diagnosing a memory system including a plurality of memory system devices, the software embodied in computer readable media and when executed operable to:

select at least one memory system device for isolation (*Fig. 1; column 4 lines 3-4, where the retainment is interpreted as isolation*);

facilitate isolation of the at least one selected memory system device (*Fig. 1; column 4 lines 3-4, memory 20a*) by disabling all system memory devices except the at least one selected memory device (*Fig. 1; column 4 lines 3-6, where the relinquishment is interpreted as disabling memory portion 20b from being tested*) or disabling the at least one selected memory device

(column 4 lines 3-22, where retaining of a portion of memory is interpreted as disabling of that portion of memory from being used by the operating system); and

perform at least one diagnostic test on the isolated device *(Fig. 2; column 4 lines 14-22)*.

As in claim 2, Schelling discloses repeating the select, facilitate and perform operations for each memory system device *(column 4 lines 14-22, where each portion of memory is interpreted as a memory system device)*.

As in claim 6, Schelling discloses if a plurality of memory system devices are selected for isolation, repeat the select, facilitate and perform operations for each device within the isolated memory system device plurality *(column 4 lines 14-22, where each portion of memory is interpreted as a memory system device; column 6 lines 35-56, multiple device testing)*.

As in claim 10, Schelling discloses software for managing a memory system having a plurality of memory system devices, the software embodied in computer readable media and when executed operable to:

receive an operating state selection for a selected memory system device *(Fig. 2; column 4 lines 34-47, where a memory portion available for test is interpreted as being in a retained operating state)*;

alter a current memory system device operating state in accordance with the operating state selection *(column 4 lines 10-22, where it is necessary to alter the state of the memory in order to test the memory)*; and

disable the selected memory system device (*column 4 lines 3-22, where retaining of a portion of memory is interpreted as disabling of that portion of memory from being used by the operating system*).

As in claim 11, Schelling discloses communicating an operating state for each memory system device (*column 4 lines 3-47, where it is necessary for communication to occur regarding an operating state [retained/relinquished] in order for the BIOS to either test or release a portion of memory*).

As in claim 12, Schelling discloses maintaining the selected operating state through subsequent information handling system boot operations (*column 3 line 48 through column 4 line 54, where it is interpreted that the relinquished state is maintained to allow relinquished processors to operate while the BIOS tests retained memory portions*).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schelling in view of Stern et al. (U.S. Patent No. 7,000,159).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention “by another”; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As in claim 3, Schelling teaches the limitations of claim 1. However, Schelling fails to teach of logging results of a diagnostic test. Stern et al. teaches of logging results of memory testing (*column 4 lines 27-28*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the logging as taught by Stern et al. in the invention of Schelling. This

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would have been obvious because the invention of Stern et al. reduces the overall time to boot a computer system while testing memory using the BIOS (*column 2 lines 41-49*).

* * *

4. Claims 4 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schelling in view of Gilbert et al. (U.S. PGPub 2004/0199830).

As in claim 4, Schelling teaches of the limitations of claim 1, including determination of a fault (*column 7 lines 6-7*). However, Schelling fails to teach of maintaining isolation of a faulty memory device. Gilbert et al. teaches of maintaining isolation of a faulty memory device (*paragraphs [0016]-[0018] and [0022]-[0023]*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the memory isolation as taught by Gilbert et al. in the invention of Schelling. This would have been obvious because the invention of Gilbert et al. reducing the amount of time necessary to repair a memory fault (*paragraphs [0005]-[0007]*).

As in claim 28, Schelling teaches of the limitations of claim 22, including determination of a fault (*column 7 lines 6-7*) and a BIOS utility which carries out the testing. However, Schelling fails to teach of maintaining isolation of a faulty memory device. Gilbert et al. teaches of maintaining isolation of a faulty memory device (*paragraphs [0016]-[0018] and [0022]-[0023]*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the memory isolation as taught by Gilbert et al. in the invention of Schelling. This would have been obvious because the invention of Gilbert et al. reducing the amount of time necessary to repair a memory fault (*paragraphs [0005]-[0007]*).

* * *

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schelling in view of Lin et al. (U.S. Patent No. 6,421,798).

As in claim 5, Shelling teaches of the limitations of claim 1. However, Schelling fails to teach of reporting a faulty operation upon testing of memory. Lin et al. teaches of reporting faulty operation (*column 7 line 66 through column 8 line 3*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the fault reporting as taught by Lin et al. in the invention of Schelling. This would have been obvious because the invention of Lin et al. reduces the time it takes to test a system by inhibiting interrupts during memory tests (*column 2 lines 29-30*).

* * *

6. Claims 7, 14, 15, 17, 18, 19, 21, 22, 24, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schelling in view of Official Notice.

As in claim 7, Schelling teaches of effecting the select, facilitate and perform operations on at least one memory of the memory system (*column 2 lines 16-20 and column 4 lines 14-22*).

However, Schelling fails to teach of a memory slot. The Examiner takes Official Notice that it is well-known in the art for memories such as RAM, DRAM, SDRAM, SRAM, and RDRAM to be included in an information handling system (such as a computer containing a motherboard) by attaching to memory slots. Further, the Examiner also takes Official Notice that it is well-known in the art for a plurality of memory slots to be included in an information handling system in order to allow for greater memory resources, improving the overall processing speed and efficiency of such an information handling system.

As in claim 14, Schelling teaches of disabling a memory card slot of the memory system, the memory card slot adapted to support a dual-channel memory card (*column 2 lines 16-20 and column 4 lines 3-22, where retaining of a portion of memory is interpreted as disabling of that portion of memory from being used by the operating system; a Rambus® DRAM is interpreted as a dual-channel memory card [see included Rambus® non-patent literature]*).

However, Schelling fails to teach of a memory slot. The Examiner takes Official Notice that it is well-known in the art for memories such as RAM, DRAM, SDRAM, SRAM, and RDRAM to be incorporated on “memory cards” and included in an information handling system (such as a computer containing a motherboard) by attaching to memory slots. Further, the Examiner also takes Official Notice that it is well-known in the art for a plurality of memory slots to be included in an information handling system in order to allow for greater memory

resources, improving the overall processing speed and efficiency of such an information handling system.

As in claim 15, Schelling teaches an information handling system, comprising:

a plurality of memory operable in at least one of a plurality of operating states (*Figs. 1 and 2; column 2 lines 16-20 and column 4 lines 34-54, where the portions of memory are interpreted as a plurality of memory, and the plurality of operating states are interpreted as “retained” and “relinquished”*);

at least one processor operably coupled to the memory (*Fig. 1; column 3 lines 62-64*);
and

a program of instructions embodied in computer readable media and executable by the processor, the program of instructions operable to effect a selected operating state for at least one of the plurality of memory (*column 4 lines 10-22, where it is necessary to alter the state of the memory in order to test the memory*); and

selectively toggle the operating state for each of the plurality of memory between enabled and disabled (*column 4 lines 3-54, where toggling between a “retained” and “relinquished” operating state is interpreted as toggling between disabled and enabled, respectively, for utilization by the operating system*).

However, Schelling fails to teach of a memory slot. The Examiner takes Official Notice that it is well-known in the art for memories such as RAM, DRAM, SDRAM, SRAM, and RDRAM to be included in an information handling system (such as a computer containing a motherboard) by attaching to memory slots. Further, the Examiner also takes Official Notice

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that it is well-known in the art for a plurality of memory slots to be included in an information handling system in order to allow for greater memory resources, improving the overall processing speed and efficiency of such an information handling system.

As in claim 17, Schelling teaches of a basic input/output system memory operably coupled to the processor (*Fig. 1 #s 12 and 14; column 2 lines 21-63*);

a basic input/output system program stored in the basic input/output system memory (*Fig. 1 #s 12 and 14; column 2 lines 21-63*); and

the program of instructions incorporated in the basic input/output system program (*Fig. 1 #s 12 and 14; column 2 lines 21-63*).

As in claim 18, Schelling teaches the program of instructions operable to maintain the selected operating state of the memory devices through additional information handling system operations (*column 3 lines 47-61*).

As in claim 19, Schelling teaches the program of instructions is operable to initiate a diagnostic routine, the diagnostic routine operable to test at least one enabled memory slot (*column 4 lines 3-22*).

As in claim 21, Schelling teaches the program of instructions operable to prevent communication with a memory module disposed in a memory slot in the disabled operating state (*column 4 lines 10-14, where it is interpreted that the "retained" memory portion is disabled*

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from being accessed by the operating system, and is therefor prevented from communication with the operating system).

As in claim 22, Schelling teaches of a method for identifying faulty devices in a memory system including a plurality of memory slots and a plurality of memory modules disposed in at least a portion of the plurality of memory and wherein the memory are controllable from a basic input-output system (BIOS) utility, comprising:

selecting a memory system device for isolation (*Fig. 1; column 4 lines 3-4, where the retainment is interpreted as isolation*);

isolating, via a BIOS utility setting, the memory system device (*Fig. 1; column 4 lines 3-4, where the retainment is interpreted as isolation*);

disabling any remaining memory system devices via the BIOS utility setting (*Fig. 1; column 4 lines 3-6, where the relinquishment is interpreted as disabling memory portion 20b from being tested*); and

performing at least one diagnostic test on the isolated memory system device, the diagnostic test operable to produce at least one result (*Fig. 2; column 4 lines 14-22 and column 7 lines 6-7*).

However, Schelling fails to teach of a memory slot. The Examiner takes Official Notice that it is well-known in the art for memories such as RAM, DRAM, SDRAM, SRAM, and RDRAM to be included in an information handling system (such as a computer containing a motherboard) by attaching to memory slots. Further, the Examiner also takes Official Notice that it is well-known in the art for a plurality of memory slots to be included in an information

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handling system in order to allow for greater memory resources, improving the overall processing speed and efficiency of such an information handling system.

As in claim 23, Schelling teaches selecting a memory system device for isolation (*Fig. 1; column 4 lines 3-4, where the retainment is interpreted as isolation*);

and disabling any remaining memory system devices via the BIOS utility setting (*Fig. 1; column 4 lines 3-6, where the relinquishment is interpreted as disabling memory portion 20b from being tested*).

As in claim 24, Schelling teaches repeating the selecting, disabling and performing operations for each memory system device (*column 4 lines 3-47*).

As in claim 25, Schelling teaches performing diagnostic testing on a memory module associated with the isolated memory system device (*column 4 lines 3-22*).

As in claim 26, Schelling teaches performing diagnostic testing on the memory slot associated with the isolated memory system device (*column 4 lines 3-47*).

* * *

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schelling in view of Official Notice, further in view of Mamata et al. (U.S. Patent No. 6,792,561).

As in claim 16, Schelling teaches of the limitations of claim 15. However, Schelling fails to teach of the remaining limitations of claim 16. Mamata teaches displaying a memory slot representation corresponding to a respective one of the plurality of memory slots (*column 6 lines 30-48*); and

communicate an operating status for each displayed memory slot representation, the operating status corresponding to an operating state for each respective memory slot (*column 6 lines 30-48*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the display aspects as taught by Mamata in the invention of Schelling. This would have been obvious because the invention of Mamata uses a BIOS application to similarly determine operating states of a memory to prevent a fault (*column 2 lines 14-15*).

* * *

8. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schelling in view of Official Notice, further in view of Lin et al.

As in claim 27, Shelling teaches of the limitations of claim 22. However, Schelling fails to teach of reporting a faulty operation upon testing of memory. Lin et al. teaches of reporting faulty operation (*column 7 line 66 through column 8 line 3*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the fault reporting as taught by Lin et al. in the invention of Schelling. This would have been obvious because the invention of Lin et al. reduces the time it takes to test a system by inhibiting interrupts during memory tests (*column 2 lines 29-30*).

* * *

9. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schelling in view of Official Notice, further in view of Lin et al., further in view of Stern et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the

reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As in claim 29, Schelling teaches the limitations of claim 22. However, Schelling fails to teach of logging results of a diagnostic test. Stern et al. teaches of logging results of memory testing (*column 4 lines 27-28*). Lin et al. teaches of reporting faulty operation (*column 7 line 66 through column 8 line 19*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the logging as taught by Stern et al. in the invention of Schelling. This would have been obvious because the invention of Stern et al. reduces the overall time to boot a computer system while testing memory using the BIOS (*column 2 lines 41-49*).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the fault reporting as taught by Lin et al. in the combined invention of Schelling and Stern et al. This would have been obvious because the invention of Lin et al. reduces the time it takes to test a system by inhibiting interrupts during memory tests (*column 2 lines 29-30*).

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PFC
10/13/2006


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